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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,615	02/26/2004	Anoop Mukker	42PI8615	6486
7590	02/27/2006			EXAMINER
Sanjeet K. Dutta Blakely, Sokoloff, Taylor & Zafman LLP 7th Floor 12400 Wilshire Boulevard Los Angeles, CA 90025			KIM, HONG CHONG	
			ART UNIT	PAPER NUMBER
			2185	
DATE MAILED: 02/27/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/788,615	MUKKER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 26 February 2004.

2a) This action is FINAL.                  2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-23 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 26 February 2004 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**Detailed Action**

1. Claims 1-23 are presented for examination. This office action is in response to the application filed on 2/26/2004.

***Information Disclosure Statement***

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search.

This request is not intended to interfere with or go beyond that required under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information

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disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

**The examiner also requests**, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1, 7, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Riedlinger et al. (Riedlinger) US Patent No. 6,647,464.

As to claims 1 and 13, Riedlinger discloses a method comprising: splitting a cache operation into two or more phases and two or more clock domains (Fig. 2).

As to claim 7, Riedlinger further disclose a cache memory array (col. 6 line 1); and control logic coupled to the cache memory array, wherein the control logic divides a cache operation into two or more phases and two or more clock domains (Fig. 2).

### ***Claim Rejections - 35 USC '103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2–6, 8-10, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riedlinger et al. (Riedlinger) US Patent No. 6,647,464 in view of Favor US Patent No. 6,732,236.

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As to claims 2, 8, and 14, Riedlinger discloses the invention as claimed above.

Riedlinger further discloses receiving the cache operation at a cache, wherein the cache operation requests data (Fig. 2 Ref 0); and returning a cache hit in response to the cache operation (col. 7 lines 50-60), however, although Riedlinger disclose pipe stage operation (col. 6 lines 35-55), Riedlinger does not specifically disclose the cache has a pending fetch for the data in response to a prior cache operation requesting the data.

Favor discloses the cache has a pending fetch for the data in response to a prior cache operation requesting the data (col. 1 lines 53-59) for the purpose of providing out of order and non sequential cache request operation thereby increasing access speed and data bandwidth.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the cache has a pending fetch for the data in response to a prior cache operation requesting the data as shown in Favor into the invention of Riedlinger for the advantages stated above.

As to claim 9, Riedlinger and Favor disclose the invention as claimed above.

Favor further discloses the control logic further comprises: a decoder connected to the cache memory array; and a controller connected to the decoder (col. 2 lines 7-23).

As to claims 3, 10, and 15, Riedlinger and Favor disclose the invention as claimed above. Favor further discloses where in response to the prior cache operation,

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the data has been requested from memory but has not yet been stored in the cache at a time when the cache receives the cache operation (col. 1 lines 53-59)

As to claims 4 and 16, Riedlinger and Favor disclose the invention as claimed above. Riedlinger further discloses the cache operation includes a tag field maintained in a first phase of the two or more phases and a data field in a second phase of the two or more phases (Fig. 2).

As to claims 5 and 17, Riedlinger and Favor disclose the invention as claimed above. Riedlinger further the cache operation includes a tag field maintained in a first clock domain of the two or more clock domains and a data field in a second clock domain of the two or more clock domains (Fig. 2).

As to claims 6 and 18, Riedlinger and Favor disclose the invention as claimed above. Riedlinger further returning the data from the cache once the data is available (col. 7 lines 48+).

4. Claims 11-12 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riedlinger et al. (Riedlinger) US Patent No. 6,647,464 in view of Favor US Patent No. 6,732,236 and further in view of Intel 865PE/865P Chipset Datasheet, Intel 865PE/865P Memory controller Hub (MCH), May 2003.

As to claim 11, Riedlinger and Favor disclose the invention as claimed above.

However, neither Riedlinger nor Favor discloses a DRAM controller integrated with the cache memory array..

Intel discloses a DRAM controller integrated with the cache memory array (Fig. 2) for the purpose of decreasing foot print thereby decreasing power and increasing access speed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a DRAM controller integrated with the cache memory array as shown in Intel into the combined invention of Riedlinger and Favor for the advantages stated above.

As to claim 12, Riedlinger, Favor, and Intel disclose the invention as claimed above. Intel further discloses an integrated graphics controller, a host AGP controller, and an I/O hub interface (Fig. 2).

As to claim 19, Riedlinger, Favor, and Intel disclose the invention as claimed above. Intel further discloses a system memory controller (Fig. 2), comprising a cache memory array (page 19), and control logic coupled to the cache memory array (Fig. 2). Riedlinger further discloses wherein the control logic divides a cache operation into two or more phases and two or more clock domains; and system memory connected to the system memory controller (Fig. 2).

As to claim 20, Riedlinger, Favor, and Intel disclose the invention as claimed above. Intel further discloses one or more interfaces connected to the system memory controller, including an I/O hub interface connected to a bus, a processor interface; and a host AGP controller connected to the system memory controller via the bus (Fig. 2). Riedlinger further discloses the cache array receives the cache operation requesting data via the one or more interfaces (Fig. 2 Ref 0); and returns a cache hit in response to the cache operation (col. 7 lines 50-60). Favor further discloses cache has a pending fetch for the data in response to a prior cache operation requesting the data (col. 1 lines 53-59).

As to claim 21, Favor further discloses where in response to the prior cache operation, the data has been requested from memory but has not yet been stored in the cache at a time when the cache receives the cache operation (col. 1 lines 53-59)

As to claim 22, Riedlinger further discloses the cache operation includes a tag field maintained in a first phase of the two or more phases and a data field in a second phase of the two or more phases (Fig. 2).

As to claim 23, Riedlinger further the cache operation includes a tag field maintained in a first clock domain of the two or more clock domains and a data field in a second clock domain of the two or more clock domains (Fig. 2).

***Conclusion***

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.
  
2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).
  
3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).
  
4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.
  
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.  
  
If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**or faxed to TC-2100:**  
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK  
Primary Patent Examiner  
February 17, 2006

*idj CL*